CLAIM AMENDMENTS

Please cancel claims 18 and 25 without prejudice or disclaimer.

Please amend claims 8, 12, 16, and 19-24 as follows.

1. (Original) An apparatus, comprising:

circuitry coupled to receive a clock signal having a frequency *f* and to output a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal, the circuitry coupled to receive a complementary clock signal having a duty cycle of approximately fifty percent and the frequency *f* and to output a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal; and

an exclusive OR circuit coupled to receive the first, second, third, and fourth signals and to output a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*.

2. (Original) The apparatus of claim 1, further comprising a buffer circuit coupled between the clock generator and each of the first, second, third, and fourth divide-by-two circuits.

3. (Original) The apparatus of claim 1, wherein the circuitry comprises:

a first divide-by-two circuit coupled to receive the first signal and preset to logic "0";

a second divide-by-two circuit coupled to receive the second signal and preset to;

a third divide-by-two circuit coupled to receive the third signal and preset to logic "0"; and

a fourth divide-by-two circuit coupled to receive the fourth signal and preset to logic "1".

4. (Original) The apparatus of claim 3, wherein the exclusive OR circuit comprises:

a first NAND gate coupled to receive the first signal and the fourth signal and to change output state from logic "1" to logic "0" when the first and fourth signals are logic "1", and to change output state from logic "0" to logic "1" when the first and fourth signals are logic "0";

a second NAND gate coupled to receive the second signal and the third signal and to change output state from logic "1" to logic "0" when the second and third signals are logic "1", and to change output state from logic "0" to logic "1" when the second and third signals are logic "0"; and

a third NAND gate coupled to receive the first NAND gate output states and the second NAND gate output states and to output the second clock.

5. (Original) The apparatus of claim 4, wherein the exclusive OR circuit further comprises:

a first set of inverters coupled to receive the first signal and apply the first signal to a first input of a fourth NAND gate and a first input of a fifth NAND gate; and

a second set of inverters coupled to receive the fourth signal and apply the fourth signal to a second input of a fourth NAND gate and a second input of a fifth NAND gate , the fourth and fifth NAND gates to change output state from 1 to 0 when the first and fourth signals have the same logic value of 1.

6. (Original) The apparatus of claim 5, wherein the exclusive OR circuit further comprises:

a third set of inverters coupled to receive the third signal and apply the third signal to a first input of a sixth NAND gate and a first input of a seventh NAND gate; and

a fourth set of inverters coupled to receive the second signal and apply the second signal to a second input of a sixth NAND gate and a second input of a seventh NAND gate, the sixth and seventh NAND gates to change output state from 1 to 0 when the second and third signals have the same logic value of 1.

7. (Original) The apparatus of claim 6, wherein the exclusive OR circuit further comprises:

an eighth NAND gate coupled to receive the fourth, fifth, sixth, and seventh NAND output states and to change output state from 1 to 0 when the fourth, fifth, sixth, and seventh NAND output states have the same logic value of 1; and

a ninth NAND gate coupled to receive the fourth, fifth, sixth, and seventh NAND output states and to change output state from 1 to 0 when the fourth, fifth, sixth, and seventh NAND output states have the same logic value of 1.

8. (Currently Amended) A method, comprising:

receiving a clock signal having a frequency *f*; [and]

outputting a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal;

receiving ~~the clock signal's~~ a complementary clock signal for the clock signal; [and]

outputting a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal; [and]

receiving the first, second, third, and fourth signals; and

outputting a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*.

9. (Original) The method of claim 8, further comprising buffering the clock signal and buffering the complementary clock signal.

10. (Original) The method of claim 8, further comprising:

dividing the frequency *f* of the clock signal by two; and

dividing the frequency *f* of the complementary clock signal by two.

11. (Original) The method of claim 10, further comprising:

exclusive OR-ing the first, second, third, and fourth signals with each other.

12. (Currently Amended) A system, comprising:

circuitry coupled to receive a clock signal having a frequency *f* and to output a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal, the circuitry coupled to receive a complementary clock signal having a duty cycle of approximately fifty percent and the frequency *f* and to output a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal;

an exclusive OR circuit coupled to receive the first, second, third, and fourth signals and to output a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*;

~~a microprocessor coupled to receive the second clock signal;~~ and

a static random access memory (SRAM) coupled to the ~~microprocessor~~ circuitry.

13. (Original) The system of claim 12, further comprising a clock generator coupled to generate the clock signal and the complementary clock signal and to provide the clock signal and the complementary clock signal to the circuitry.

14. (Original) The system of claim 13, wherein the clock generator comprises a phase-locked loop clock generator.

15. (Original) The system of claim 14, wherein the phase-locked loop clock generator comprises a voltage-controlled oscillator.

16. (Currently Amended) A method, comprising:

receiving a first clock signal and its complementary clock signal from a first power domain, the clock signal and the complementary clock signal each having a duty cycle of approximately fifty percent and a frequency *f*;

dividing the frequency *f* of the clock signal by two in a second power domain;

dividing the frequency *f* of the complementary clock signal by two in the second power domain; [and]

exclusive OR-ing the divided-by-two clock signal and the divided-by-two complementary clock signal in the second power domain to generate a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*;

outputting a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal;

outputting a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal; and

receiving the first, second, third, and fourth signals and outputting a second clock signal having a duty cycle of approximately fifty percent and the frequency.

17. (Original) The method of claim 16, further comprising:

buffering the clock signal in the second power domain; and

buffering the complementary clock signal in the second power domain.

18. (Canceled).

19. (Currently Amended) An article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising the method of:

receiving a clock signal having a frequency *f* and outputting a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal;

receiving ~~the clock signal's~~ a complementary clock signal for the clock signal and outputting a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal; and

receiving the first, second, third, and fourth signals and outputting a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*.

20. (Currently Amended) The article of manufacture of claim 19, wherein the ~~machine-accessible medium further includes~~ data ~~that~~ is further to cause the machine to perform operations comprising buffering the clock signal and buffering the complementary clock signal.

21. (Currently Amended) The article of manufacture of claim 19, wherein the ~~machine-accessible medium further includes~~ data ~~that~~ is further to cause the machine to perform operations comprising:

dividing the frequency *f* of the clock signal by two; and

dividing the frequency *f* of the complementary clock signal by two.

22. (Currently Amended) The article of manufacture of claim 21, wherein the ~~machine-accessible medium further includes~~ data ~~that~~ is further to cause the machine to perform operations comprising exclusive OR-ing the first, second, third, and fourth signals with each other.

23. (Currently Amended) An article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving a first clock signal and its complementary clock signal from a first power domain, the clock signal and the complementary clock signal each having a duty cycle of approximately fifty percent and a frequency *f*;

dividing the frequency *f* of the clock signal by two in a second power domain;

dividing the frequency *f* of the complementary clock signal by two in the second power domain; [and]

exclusive OR-ing the divided-by-two clock signal and the divided-by-two complementary clock signal in the second power domain to generate a second clock signal having a duty cycle of approximately fifty percent and the frequency *f*;

outputting a first signal in phase with the clock signal at one-half the frequency *f* and a second signal one hundred eighty degrees out of phase with the first signal;

outputting a third signal ninety degrees out of phase with the first signal and a fourth signal one hundred eighty degrees out of phase with the third signal; and

receiving the first, second, third, and fourth signals and outputting a second clock signal having a duty cycle of approximately fifty percent and the frequency.

24. (Currently Amended) The article of manufacture of claim 23, wherein the ~~machine-accessible medium further includes~~ data ~~that~~ is further to cause the machine to perform operations comprising:

buffering the clock signal in the second power domain; and

buffering the complementary clock signal in the second power domain.

25. (Canceled).